What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A method of forming a device to be used in a memory array, the device comprising a gate structure provided on a surface of a semiconductor substrate, said method comprising the steps of:

forming a first doping implant within the substrate to form first and second diffusion regions underneath the surface of the substrate on opposite sides of the gate structure;

forming a second doping implant within the substrate at locations of the first and second diffusion regions to add additional dopant to the first and second diffusion regions, wherein each diffusion region comprises a first portion having a first dopant concentration and a second portion having a second dopant concentration.

2. The method of claim 1 wherein the dopant is selected from the group consisting of phosphorous, arsenic and antimony.

3. The method of claim 2 wherein the dopant is phosphorous.

4. The method of claim 1 wherein said first doping implant step is performed at a first energy level and first dose and said second doping implant is performed at a second energy level and second dose.

5. The method of claim 4 wherein the first energy level is different from the second energy level.

6. The method of claim 4 wherein the first dose is different from the second dose.

7. The method of claim 4 wherein the first energy level is less than 30 Kev and the first dose is less than $7x10^{12}$ ions/cm^2.

8. The method of claim 4 wherein the first energy level is within a range of 5 Kev to 45 Kev and the first dose is within a range of $1x10^{12}$ ions/cm^2 to less than $7x10^{12}$ ions/cm^2.

9. The method of claim 4 wherein the first energy level is approximately 15 Kev and the first dose is approximately $2x10^{12}$ ions/cm^2.

10. The method of claim 4 wherein the second energy level is less than 30 Kev and the second dose is less than $1x10^{13}$ ions/cm^2.

11. The method of claim 4 wherein the second energy level is within a range of 5 Kev to 60 Kev and the second dose is within a range of $1x10^{12}$ ions/cm^2 to $1x10^{13}$ ions/cm^2.

12. The method of claim 4 wherein the second energy level is approximately 20 Kev and the second dose is approximately $4x10^{12}$ ions/cm^2.

13. The method of claim 1 wherein the first dopant concentration is different from the second dopant concentration.

14. The method of claim 1, wherein said first and second doping implants are performed by blanket ion implanting process.

15. The method of claim 14, wherein sidewalls of the gate structure are oxidized prior to said second doping implant.

16. The method of claim 15, wherein the sidewalls of the gate structure are oxidized by e thermal re-ox process.

17. A method of forming a metal oxide semiconductor field effect transistor comprising the steps of:

providing a gate structure on a surface of a semiconductor substrate;

implanting a dopant within the substrate to form first and second diffusion regions underneath the surface of the substrate;

oxidizing sidewalls of the gate structure; and

implanting the dopant within the substrate at locations of the first and second diffusion regions to add additional dopant to the first and second diffusion

regions, wherein each diffusion region comprises a first portion having a first dopant concentration and a second portion having a second dopant concentration.

18. A method of forming a device on a substrate, the device comprising a gate structure provided on a surface of the substrate, said method comprising the steps of:

implanting a dopant at a first energy level and first dose into the substrate to form first and second diffusion regions underneath the surface of the substrate on opposite sides of the gate structure; and

implanting the dopant at a second energy level and second dose into the substrate at locations of the first and second diffusion regions to add additional dopant to the first and second diffusion regions, wherein each diffusion region comprises a first portion having a first dopant concentration and a second portion having a second dopant concentration.

19. The method of claim 18 wherein the dopant is selected from the group consisting of phosphorous, arsenic and antimony.

20. The method of claim 19 wherein the dopant is phosphorous.

21. The method of claim 18 wherein the first energy level is different from the second energy level.

22. The method of claim 18 wherein the first dose is different from the second dose.

23. The method of claim 18 wherein the first energy level is less than 30 Kev and the first dose is less than $7x10^{12}$ ions/cm^2.

24. The method of claim 18 wherein the first energy level is within a range of 5 Kev to 45 Kev and the first dose is within a range of $1x10^{12}$ ions/cm^2 to less than $7x10^{12}$ ions/cm^2.

25. The method of claim 18 wherein the first energy level is approximately 15 Kev and the first dose is approximately $2x10^{12}$ ions/cm^2.

26. The method of claim 18 wherein the second energy level is less than 30 Kev and the second dose is less than $1x10^{13}$ ions/cm^2.

27. The method of claim 18 wherein the second energy level is within a range of 5 Kev to 60 Kev and the second dose is within a range of $1x10^{12}$ ions/cm^2 to $1x10^{13}$ ions/cm^2.

28. The method of claim 18 wherein the second energy level is approximately 20 Kev and the second dose is approximately $4x10^{12}$ ions/cm^2.

29. The method of claim 18 wherein the first dopant concentration is different from the second dopant concentration.

30. The method of claim 18, wherein said implanting steps are performed by a blanket ion implanting process.

31. The method of claim 30, wherein sidewalls of the gate structure are oxidized prior to said second implanting step.

32. The method of claim 31, wherein the sidewalls of the gate structure are oxidized by a thermal re-ox process.

33. A method of forming a memory array device on a substrate, the device comprising a gate structure provided on a surface of the substrate, said method comprising the steps of:

blanket ion implanting a dopant at a first energy level and first dose into the substrate to form first and second diffusion regions underneath the surface of the substrate on opposite sides of the gate structure;

oxidizing sidewalls of the gate structure; and

blanket ion implanting the dopant at a second energy level and second dose into the substrate at locations of the first and second diffusion regions to add additional dopant to the first and second diffusion regions, wherein each diffusion region comprises a first portion having a first dopant concentration and a second portion having a second dopant concentration.

34. The method of claim 33, wherein said oxidizing step is a thermal re-ox process.

35. An integrated circuit semiconductor device comprising:

a substrate having a first surface;

a gate structure formed on said first surface; and

first and second diffusion regions formed within said substrate on opposite sides of said gate structure, wherein each of said diffusion regions comprise first and second portions respectively having first and second dopant concentrations, which are different and cause each diffusion region to have a graded dopant concentration.

36. The device of claim 35 wherein said first and second diffusion regions are doped with phosphorous.

37. The device of claim 35 wherein said first diffusion region is partially located underneath a first side wall of said gate structure and said second diffusion region is partially located underneath a second side wall of said gate structure.

38. A processor-based system comprising:

a processor; and

a memory circuit coupled to said processor, said memory circuit comprising:

a substrate having a first surface;

a gate structure formed on said first surface; and

first and second diffusion regions formed within said substrate on opposite sides of said gate structure, wherein each of said diffusion regions comprise first and second portions respectively having first and second dopant concentrations, which are different and cause each diffusion region to have a graded dopant concentration.

39. A processor-based system comprising:

a processor; and

a memory circuit coupled to said processor, said memory circuit being integrated on a same chip as said processor, said memory circuit comprising:

a substrate having a first surface;

a gate structure formed on said first surface; and

first and second diffusion regions formed within said substrate on opposite sides of said gate structure, wherein each of said diffusion regions comprise first and second portions respectively having first and second dopant concentrations, which are different and cause each diffusion region to have a graded dopant concentration.